Electronic and Signal Processing Exam

Prof. Dr. E. Chicca

Exam - April 4^{th} 2022

Problem 1 (14 points)

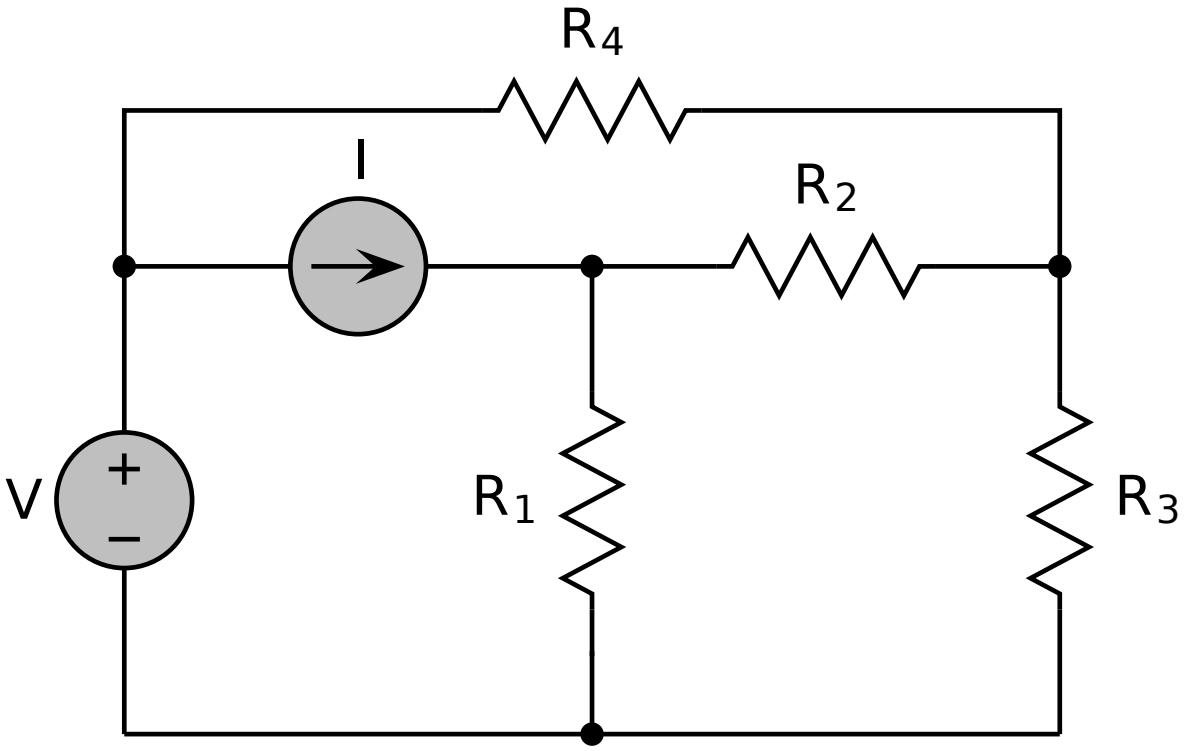


Figure 1: Resistor network.

Consider the circuit in Figure 1 and the related **parameters**: $R_1 = 2k\Omega$, $R_2 = 4k\Omega$, $R_3 = 2k\Omega$, $R_4 = 2k\Omega$, $V = 12V$, $I = 3mA$.

(a) (2 points) Clearly state the Thévenin theorem.

(b) (4 points) Determine the equivalent resistance R_{eq} seen by R_1 (consider R_1 an open circuit and calculate the resistance between the two nodes originally connected to R_1).

(c) (4 points) Determine the Thévenin equivalent voltage V_{oc} of the open circuit seen by R_1.

(d) (4 points) Compute I_{R_1} and I_{R_2}.

Problem 1 - Solution

Point a

Thévenin Theorem: Any linear electric network can be replaced by an equivalent circuit containing a single independent voltage source V_{th} and series resistance R_{th}. The theorem is applied to the network after removing the load between tow arbitrary terminals A and B. The equivalent voltage V_{th} is the voltage obtained at the terminals A-B. The equivalent resistor R_{th} is the resistance between the terminals A-B calculated after replacing all voltage sources with a short circuit and all current sources with an open circuit (e.g. replace each source with its ideal internal resistance).

Point b

We use the Thévenin theorem to find the equivalent circuit connected to R_1 (Fig. 2). We remove R_1 and compute the equivalent resistance at its nodes (Fig. 3) To do that we need to not consider the active elements, the generators. They have to be replaced by their ideal internal resistance, as shown in Fig. 3. Therefore, the equivalent resistor can be calculated as follows:

$$R_{eq} = R_2 + R_3//R_4 = R_2 + \frac{R_3 R_4}{R_3 + R_4} = 4k\Omega + \frac{2 \cdot 2}{2+2} k\Omega$$

So $R_{eq} = \underline{\underline{5k\Omega}}$.

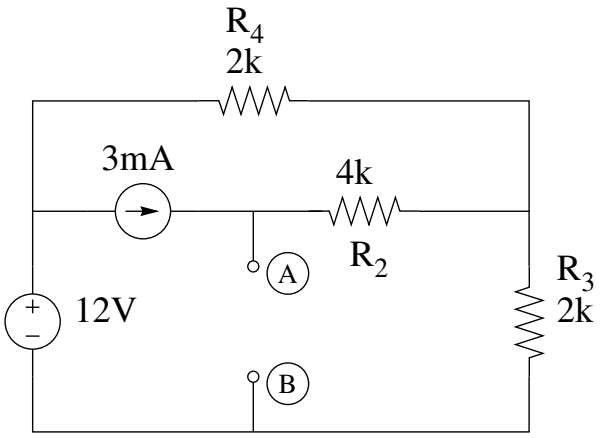


Figure 2: Thevenin Equivalent R1: Step 1.

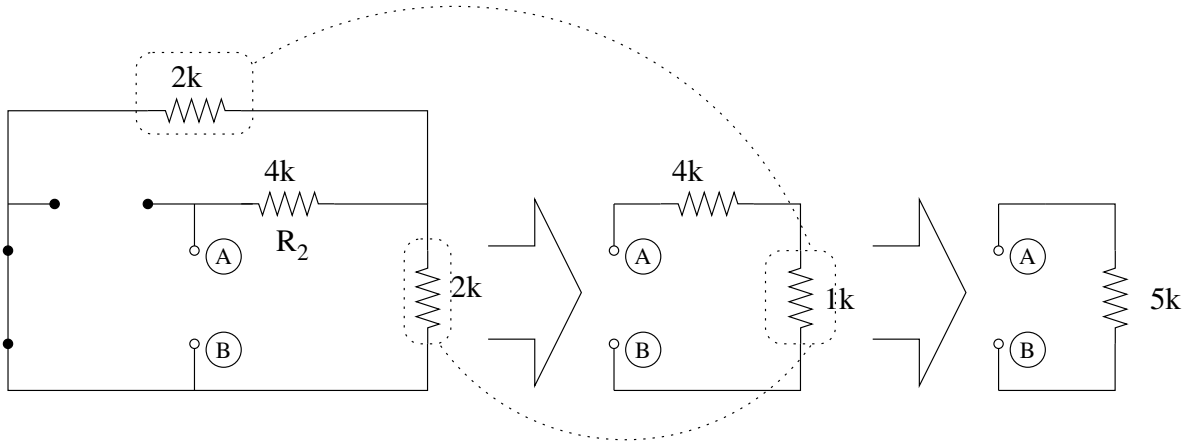


Figure 3: Thevenin Equivalent R1: Step 2.

Remarks

This question is comparable to top problem 2.2. The number and type of sources is identical (1 voltage source and 1 current source), 3 resistors instead of 5 need to be considered here (lower complexity than the top problem).

Point c

The equivalent generator can be calculated using the superposition principle.

First the current generator is kept while the voltage generator is removed (shorted) (see Fig. 4). The partial equivalent voltage is then

$$V'_{AB} = 3mA \cdot 5k\Omega = 15V$$

where $5k\Omega$ is the equivalent resistance of $R_{2,3,4}$ as calculated in b).

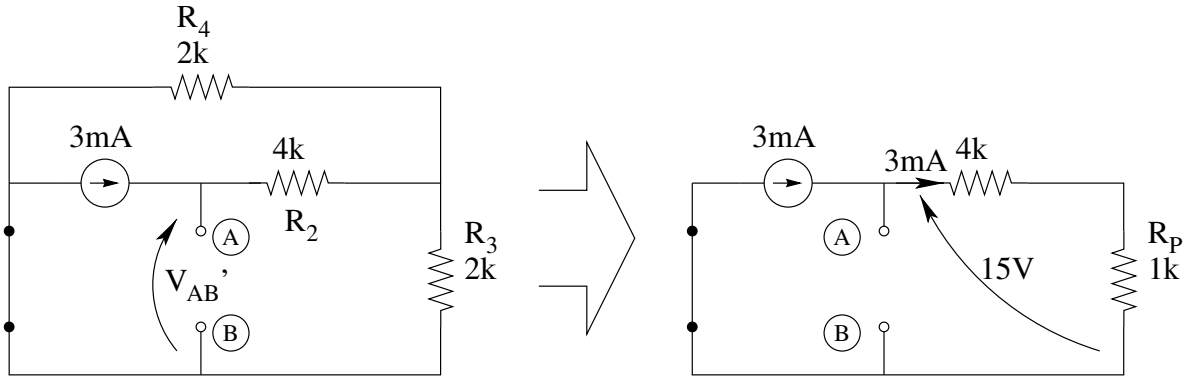


Figure 4: Thevenin Equivalent R1: Step 3.

Then the voltage generator is kept while the current generator is removed and substituted by an open circuit (Fig. 5). We first notice that the resistor R_2 cannot pass any current, since one of its nodes is then floating. The partial equivalent voltage is then obtained by applying the voltage divider equation (as in Fig. 5) composed of R_4 and R_3 only:

$$V''_{AB} = 12V \frac{2k\Omega}{2k\Omega + 2k\Omega} = 6V$$

We sum the two effects:

$$V_{eq} = V'_{AB} + V''_{AB} = 15V + 6V = \underline{\underline{21V}}$$

Remarks

This question is comparable to top problem 2.2. The number and type of sources is identical (1 voltage source and 1 current source), 3 resistors instead of 5 need to be considered here (lower complexity than the top problem).

Point d

Replacing the circuit with its Thévenin equivalent (see Fig. 6), we get

$$I_{R_1} = \frac{V_{eq}}{R_{eq} + R_1} = \frac{21V}{7k\Omega} = \underline{\underline{3mA}}$$

We can apply KCL to the node common to the current generator, R_1 and R_2 (see Fig. 1), labeled as node C in Fig. 7:

$$I = I_{R_1} + I_{R_2} \rightarrow I_{R_2} = I - I_{R_1} = 3mA - 3mA = \underline{\underline{0mA}}$$

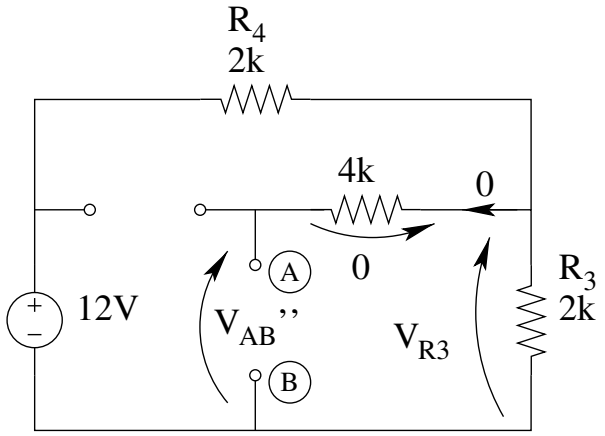


Figure 5: Thevenin Equivalent R1: Step 4.

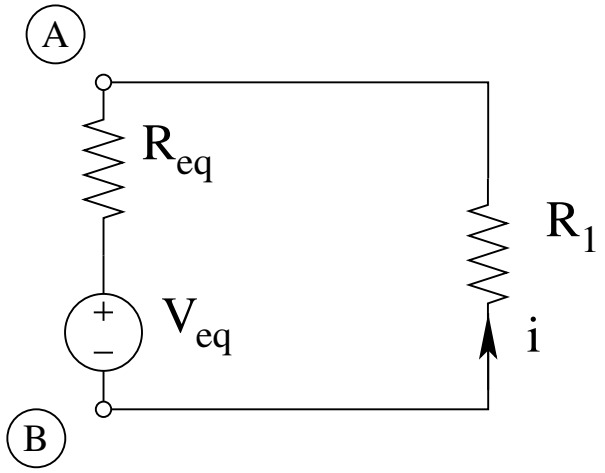


Figure 6: Thevenin Equivalent R1: Step 5.

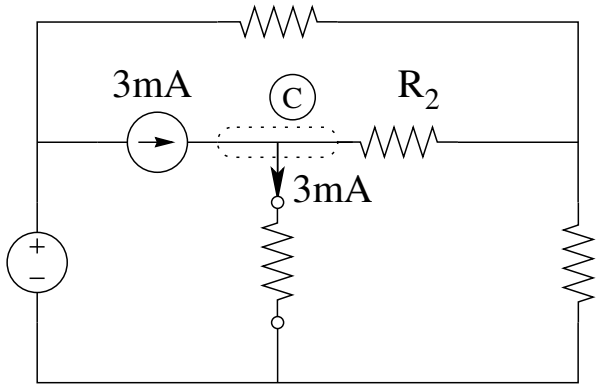


Figure 7: Current calculation R2.

Remarks

The first question can be solved with mesh analysis if b and c are not solved. The complexity is much lower than top problem 1.1 (1 voltage supply, 11 resistors). The second question is very simple and only requires to apply KCL to one node.

Problem 2 (21 points)

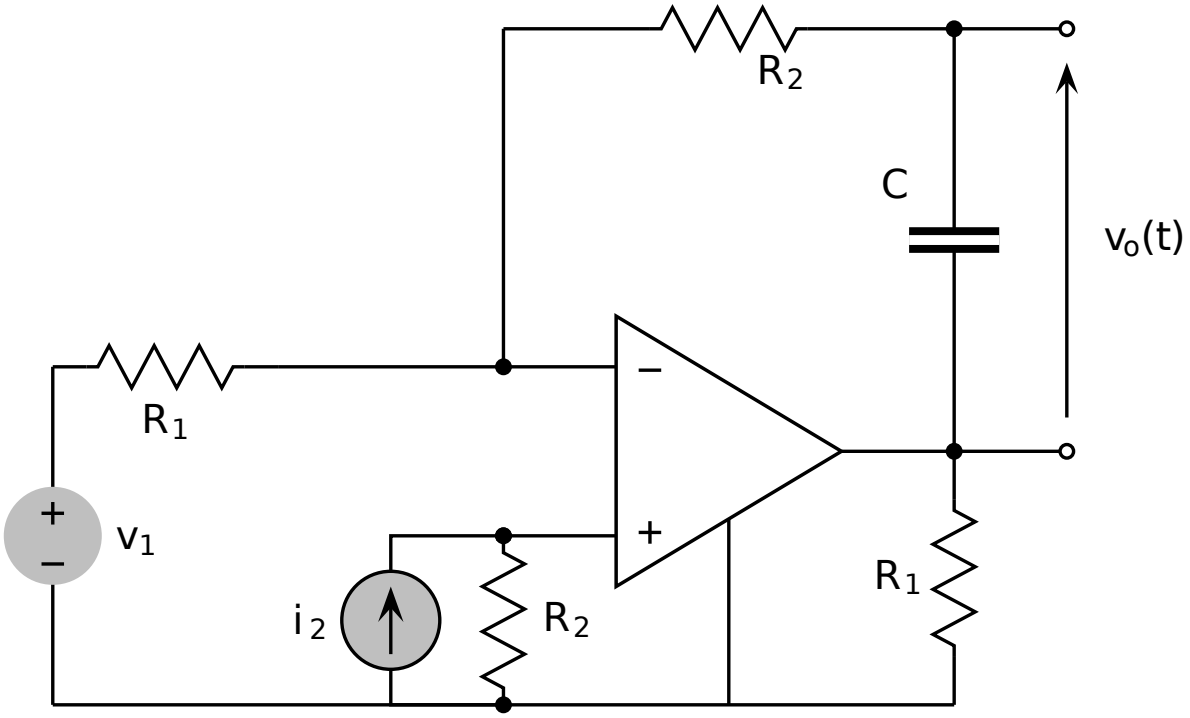


Figure 8: Circuit with OPAMP.

Consider the circuit in Figure 8. It operates in a **sinusoidal** regime with an **ideal** opamp and **ideal** components.
Parameters: $R_1 = 1k\Omega$, $R_2 = 2k\Omega$, $C = 0.5\mu F$, $\omega_0 = 1000\ rad/s$.

(a) (5 points) Using the superposition principle, derive the relation $H_1(j\omega)$ between v_0 and v_1

$$H_1(j\omega) := \frac{v_0}{v_1} = \frac{1}{R_1}\frac{1}{j\omega C}$$

(b) (5 points) ... $H_2(j\omega)$ between V_0 and I_2

$$H_2(j\omega) := \frac{v_0}{i_2} = -\frac{R_2}{R_1}\frac{1}{j\omega C}$$

(c) (8 points) Assuming $v_1(t) = 0\text{V}$, $i_2(t) = \cos(\omega_0 t)$ mA, determine $|v_0(t)|$.

(d) (3 points) Assuming $v_1(t) = 2\cos(\omega_0 t)$ V, $I_2(t) = \sin(\omega_0 t)$ mA, determine $|v_0(t)|$ in its simplest form.

Problem 2 - Solution

Point a

For obtaining the first transfer function, we replace generator 2 with its ideal equivalent resistance (open circuit, see Fig. 9). Taking the negative terminal of V_1 to be the reference voltage (0 V), the positive terminal of the opamp will be 0 V. Thus the negative terminal will be 0 V also (virtual node). The current through the leftmost R_1 thus equals $\frac{V_1}{R_1}$. Since there is no current into the terminals of the opamp (ideal), all this current goes to the capacitor. We then obtain

$$V_0 = \frac{V_1}{R_1} * \frac{1}{j\omega C}$$

.

From this we get

$$H_1(j\omega) = \frac{1}{R_1 j\omega C}$$

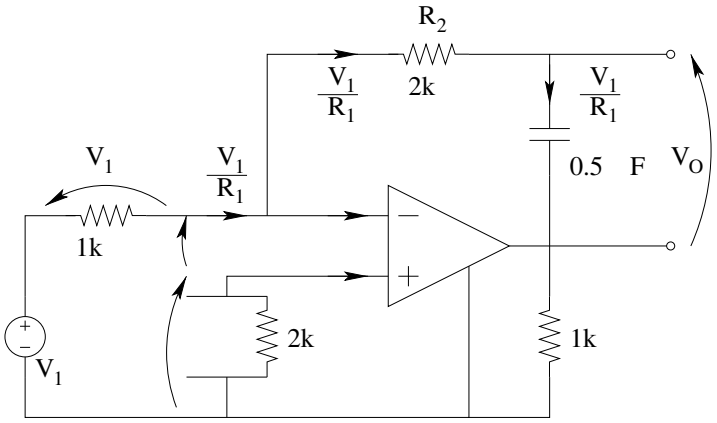


Figure 9: OPAMP network.

Remarks

Reasoning about the circuit with only the voltage source makes this question comparable to question 1 of the tutorial assignment for week 4 (see Nestor page), except that the resistor and capacitor are in series here instead of parallel. The math steps required are minimal, but a good understanding of basic principles (e.g. virtual node) is required. The final solution is provided in the hope to guide the reasoning of the students.

Point b

For the second function, we replace generator 1 with its equivalent resistance (wire, see Fig. 10). The voltage across the bottom-most R_2 is $I_2 R_2$ (and so the + terminal of the opamp). Thus the negative terminal will be $V = I_2 R_2$ also. The current through the leftmost R_1 is then $\frac{I_2 R_2}{R_1}$. Since there is no current into terminals of the opamp (ideal), all this current goes to capacitor.

We obtain

$$V_0 = I Z_{\text{cap}} = \Big(- \frac{R_2 I_2}{R_1} \Big) \frac{1}{j\omega C}$$

negative sign due to the direction of the current.

From which

$$H_2(j\omega) = -\frac{R_2}{R_1} \frac{1}{j\omega C}$$

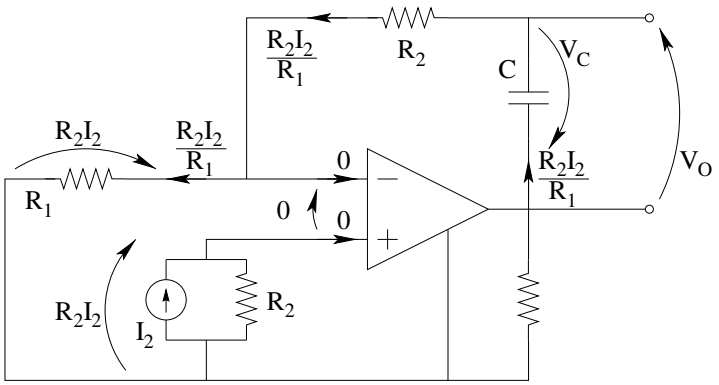


Figure 10: OPAMP network.

Remarks

The complexity of this question is also comparable to question 1 of the tutorial assignment for week 4 (see Nestor page). Knowledge about Ohm law as well as basic principles of opamp operation are clearly also required. The math steps required are minimal. The final solution is provided in the hope to guide the reasoning of the students.

Point c

We have $V_0 = H_1 V_1 + H_2 I_2 = H_2 I_2$ from superposition. Have

$$H_2 = -\frac{2}{1} * \frac{1}{j * 10^3 * 0.5 * 10^{-6}} = +4000jVA^{-1}$$

So

$$V_0(t) = H_2 \cdot i_2 = 4000j \cdot 10^{-3} e^{j\omega t}\mathrm{V} = 4 \cdot e^{j\frac{\pi}{2}} \cdot e^{j\omega t}\mathrm{V} = 4 \cdot e^{j(\omega t + \frac{\pi}{2})}\mathrm{V}$$

and taking the real part because complex voltages don't actually exist.

$$V_0(t) = 4\cos(10^3 t + \frac{\pi}{2}) = -4\sin(10^3 t)\mathrm{V}$$

Remarks

The fact that the final solution for points a and b is provided guarantees that this point can be solved by simply applying the superposition principle. The rest is simple math.

Point d

Same method as c), but now need H_1.

Substitute:

$$H_1 = \frac{1}{j10^3 \cdot 10^3 \cdot 0.5 \cdot 10^{-6}} = -2j$$

The contribution to V_0 from V_1 is thus

$$\Delta V_0(t)_{\text{from 1}} = -2j \cdot 2e^{j\omega t}V = 4 \cdot e^{j(\omega t - \frac{\pi}{2})}V$$

Since the i_2 is the same as in part c) but a sine rather than a cosine, we can just shift its contribution backwards by $\frac{\pi}{2}$ (or recalculate it):

$$\Delta V_0(t)_{\text{from 2}} = 4e^{j\omega t}V$$

Adding the two contributions, we get

$$V_0(t) = 4 \cdot e^{j(\omega t - \frac{\pi}{2})} + 4e^{j\omega t}V = 4e^{j\omega t}\big(1 + e^{-j\frac{\pi}{2}}\big) = 4e^{j\omega t}\big(1 - j\big) = 4e^{j\omega t}\big(\sqrt{2}e^{-\frac{\pi}{4}}\big)$$

Taking reals, the real voltage across C is then

$$V_0(t) = 4\sqrt{2}\cos(10^3 t - \frac{\pi}{4})V$$

The final answer is then

$$|V_0(t)| = 4\sqrt{(2)}|\cos(10^3 t - \frac{\pi}{4})|V$$

Remarks

The fact that the final solution for points a and b is provided guarantees that this point can be solved by simply applying the superposition principle. The rest is simple math.

Problem 3 (21 points)

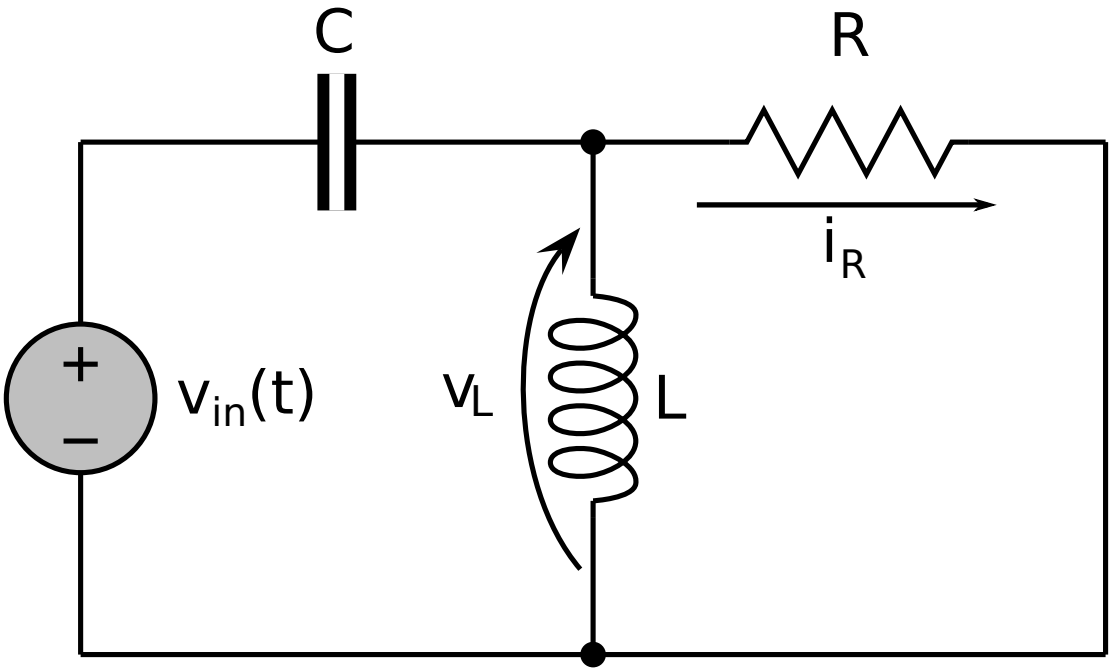


Figure 11: RLC circuit.

Consider the circuit in Figure 11. Assume **sinusoidal** regime, **ideal** components and the following **parameters**: $C = 0.25mF$, $R = 8\Omega$, $L = 0.5mH$, $\omega_0 = 2000\ rad/s$.

(a) (5 points) **Without** using any calculation, but **only** reasoning about the behavior of each element in the circuit, describe the behavior of

$$H(j\omega) := \frac{i_R}{v_{in}}$$

for low ($\omega \to 0$) and high ($\omega \to \infty$) frequencies.

(b) (16 points) Determine $v_L(t)$ considering $v_{in}(t) = -\sqrt{2}sin(\omega_0 t)\ V$ and reduce it to a similar form as given for $v_{in}(t)$ but using the cosine instead of the sine.

Problem 3 - Solution

Point a

For low frequencies ($\omega \to 0$ rad/s) the capacitor impedance $Z_C \to \infty$, while the inductor impedance $Z_L \to 0$. Thus the equivalent impedance of the parallel resistor and inductor $\to 0$, and so $\underline{\underline{H(j\omega) \to 0}}$.

For high frequencies ($\omega \to \infty$ rad/s) the capacitor impedance $Z_C \to 0$, while the inductor impedance $Z_L \to \infty$. Thus the capacitor may be replaced by a closed circuit, and the impedance contribution from the parallel inductor may be ignored. Thus the circuit resembles just a resistor, and so $\underline{\underline{H(j\omega) \to \frac{1}{R}}}$.

Point b

First we calculate the impedances of all the elements:

- $Z_C = \frac{1}{j\omega C} = -j\frac{1}{2000*0.25*10^{-3}} = -2j\Omega$
- $Z_L = j\omega L = j*2000*0.5*10^{-3} = j\Omega$
- $Z_R = R = 8\Omega$

We then need to calculate the impedance of the parallel components

$$Z_R||Z_L = \frac{Z_L Z_R}{Z_L + Z_R} = \frac{8j}{j+8}\Omega$$

We then apply the voltage divider formula

$$V_L = V_{in} \cdot \frac{Z_L||Z_R}{Z_L||Z_R + Z_C} = V_{in} \cdot \frac{\frac{8j}{j+8}}{\frac{8j}{j+8} - 2j} = V_{in} \cdot \Big[-\frac{16}{17} + \frac{4}{17}j \Big]$$

We have $V_{in}(t) = -\sqrt{2}\sin(\omega_0 t)$ so $\tilde{V}_{in}(t) = \sqrt{2}e^{j\omega_0 t + j\frac{\pi}{2}}$
Thus,

$$V_L = \sqrt{2}e^{j\omega_0 t + j\frac{\pi}{2}} \cdot \Big[-\frac{16}{17} + \frac{4}{17}j \Big]$$

What remains is to calculate the phase and magnitude of V_L:

$$\phi(V_L) = \frac{\pi}{2} + \arctan(\frac{4/17}{-16/17}) = \frac{\pi}{2} - 0.244979... = 1.32582...\text{rad}$$

$$|V_L| = \sqrt{2} \cdot |-\frac{16}{17} + \frac{4}{17}j| = \sqrt{2} \cdot \sqrt{(\frac{16}{17})^2 + (\frac{4}{17})^2} = \frac{4\sqrt{34}}{17}V$$

Taking reals, the final real voltage is then

$$V_L(t) = \underline{\underline{\frac{4\sqrt{34}}{17}\cos(\omega_0 t + 1.326\text{rad})V}} = \underline{\underline{\frac{4\sqrt{34}}{17}\cos(\omega_0 t + 75.96^\circ)V}}$$

where V_L is given as a cosine as required.

Remarks

The complexity of this problem is comparable to top problem 4 (see tutorial assignment for week 3 on Nestor).

Problem 4 (14 Points)

Legend:

$$A \cdot B = \text{AND}$$

$$A + B = \text{OR}$$

$$\overline{A} = \text{NOT A}$$

a) Logic minimisation with Karnaugh maps (4 points)

$y = (\overline{D}\cdot\overline{C}\cdot A\cdot\overline{B})+(\overline{D}\cdot C\cdot\overline{A}\cdot\overline{B})+(\overline{D}\cdot C\cdot A\cdot\overline{B})+(D\cdot C\cdot\overline{A}\cdot\overline{B})+(D\cdot C\cdot A\cdot\overline{B})+(D\cdot C\cdot A\cdot B)+(D\cdot C\cdot\overline{A}\cdot B)+(D\cdot\overline{C}\cdot A\cdot\overline{B})$

Fill out the **Karnaugh map** to represent the expression above and use it to **optimise** the logic needed to implement the given expression. Please extract the **reduced** logic formula out of the Karnaugh map and do not use algebraic simplifications.

b) Logic mapping with Boolean algebra (4 points)

$y = (A \cdot \overline{B}) + (C \cdot \overline{B}) + (D \cdot C \cdot B) + (D \cdot C \cdot A)$

You can only use 2 input NOR gates and inverters (NOT gates) to implement the provided Boolean expression. Use Boolean algebra to change the formula accordingly and draw the resulting combinational logic with NOR and INV symbols.

c) Circuit function completion (6 points)

You are given the combinational logic shown in Figure 12. Add only one inverter (NOT gate) and only one 2 input gate of your choice from AND, NAND, OR, NOR, INV to the provided logic to implement a 2 input XOR function. Draw the 2 gates on to Figure 12.

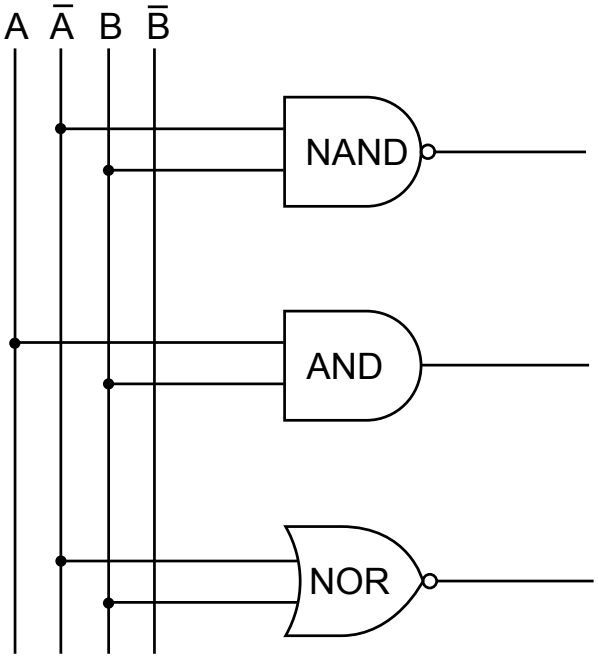


Figure 12: 3 logic gates.

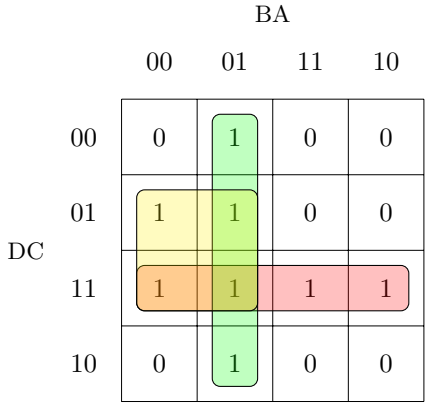
Problem 4 - Solution

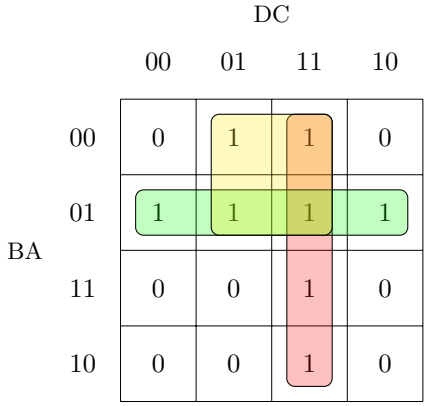
Point a

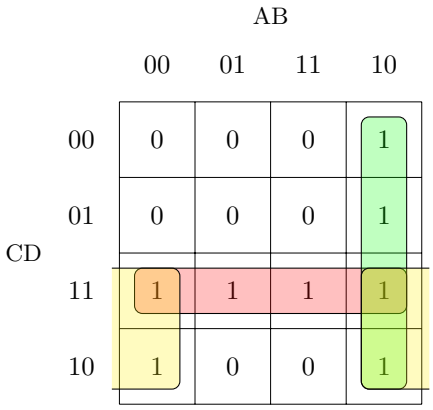
The Karnaugh map is drawn with gray code, so only one digit changes per step, with 2 variables vertical and 2 horizontal. Each of the given terms eg.

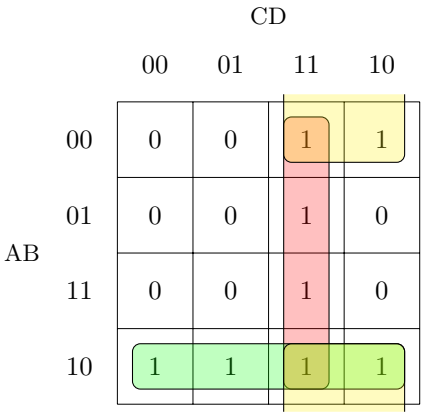
$$(\overline{D} \cdot \overline{C} \cdot A \cdot \overline{B})$$

appears as a one in the map, the rest of the positions are zero. Mark all groups of 2 (one variable reduced), 4 (two variables reduced), 8 (3 variables reduced), 16 (all variables reduced) that you can find, individual positions can be used in multiple groups. Groups can be formed over the edge.









$$y = (green) + (yellow) + (red)$$

$$y = (A \cdot \overline{B}) + (C \cdot \overline{B}) + (D \cdot C)$$

$$A \cdot B = \text{AND}$$
$$A + B = \text{OR}$$
$$\overline{A} = \text{NOT A}$$

Remarks

The Karnaugh map for this question is comparable to the one provided in the solution of exercise 24.16 of the book (provided in week 6 on Nestor). The Karnaugh maps needed for exercises 24.23 and 24.24 (part of the tutorial assignments of week 6, see Nestor and related solutions) are somewhat more complex than this one.

Point b

Variant 1

The De Morgan's laws can be used to turn all gates into 2 input NOR gates, after a first step for logic simplification.

$$y = (A \cdot \overline{B}) + (C \cdot \overline{B}) + (D \cdot C \cdot B) + (D \cdot C \cdot A)$$

simplifies to:

$$y = ((A + C) \cdot \overline{B}) + (D \cdot C \cdot (B + A))$$

First change the formula to only have 2-input gates

$$y = ((A + C) \cdot \overline{B}) + ((D \cdot C) \cdot (B + A)$$

Introduce double inversion to every inner 2 input AND expressions:

$$y = \overline{\overline{((A + C) \cdot \overline{B})}} + \overline{\overline{((D \cdot C)} \cdot (B + A)}$$

Swap gates from 2 input AND gates to 2 input NOR gates by inverting the inputs:

$$y = \overline{\overline{((A + C)} + \overline{\overline{B}})} + \overline{\overline{((\overline{D} + \overline{C})} + \overline{(B + A)}}$$

Remove obsolete double inversion on single variables:

$$y = \overline{\overline{((A + C)} + B)} + \overline{\overline{((\overline{D} + \overline{C})} + \overline{(B + A)}}$$

Add double inversion to the outer 2 input OR gate:

$$y = \overline{\overline{\overline{((A + C)} + B)}} + \overline{\overline{\overline{((\overline{D} + \overline{C})} + \overline{(B + A)}}}$$

Draw the circuit.

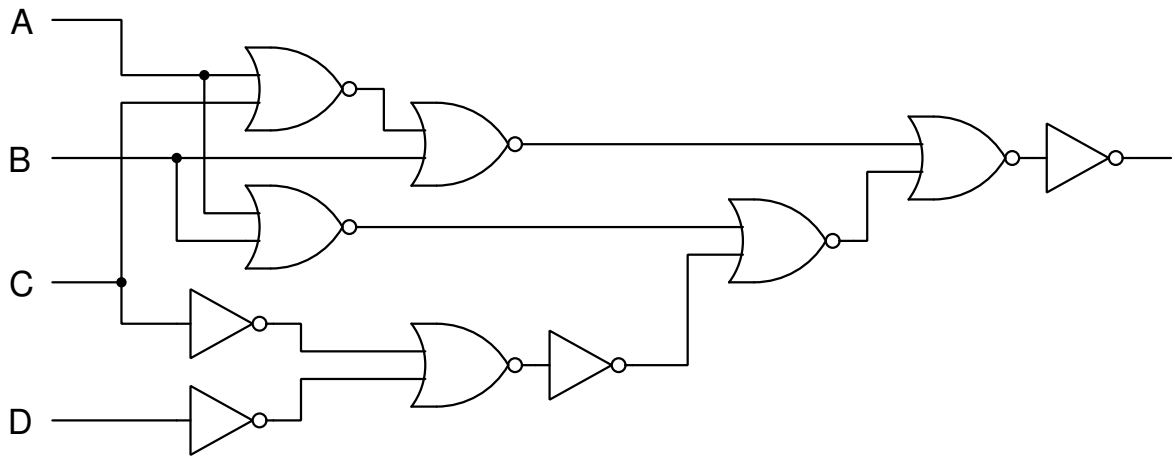


Figure 13: The 2 input NOR and INV gates circuit variant1.

Variant 2

Using De Morgan's laws turn all gates into 2 input NOR gates without logic simplification.

$$y = (A \cdot \overline{B}) + (C \cdot \overline{B}) + (D \cdot C \cdot B) + (D \cdot C \cdot A)$$

First change the formula to only have 2-input gates:

$$y = (A \cdot \overline{B}) + (C \cdot \overline{B}) + (D \cdot (C \cdot B)) + (D \cdot (C \cdot A))$$

Apply double inversion to every inner pair:

$$y = (\overline{\overline{(A \cdot \overline{B})}} + \overline{\overline{(C \cdot \overline{B})}}) + (\overline{\overline{(D \cdot \overline{\overline{(C \cdot B)}})}} + \overline{\overline{(D \cdot \overline{\overline{(C \cdot A)}})}})$$

Swap expressions from 2 input AND to 2 input NOR by inverting the inputs:

$$y = (\overline{(\overline{A} + \overline{\overline{B}})} + \overline{(\overline{C} + \overline{\overline{B}})}) + (\overline{(\overline{D} + \overline{\overline{(\overline{C} + \overline{B})}})} + \overline{(\overline{D} + \overline{\overline{(\overline{C} + \overline{A})}})})$$

Remove obsolete double inversion on single variables:

$$y = (\overline{(\overline{A} + B)} + \overline{(\overline{C} + B)}) + (\overline{(\overline{D} + \overline{\overline{(\overline{C} + \overline{B})}})} + \overline{(\overline{D} + \overline{\overline{(\overline{C} + \overline{A})}})})$$

Add double inversion to the outer 2 input OR gates:

$$y = \overline{\overline{(\overline{(\overline{A} + B)} + \overline{(\overline{C} + B)})}} + \overline{\overline{(\overline{(\overline{D} + \overline{\overline{(\overline{C} + \overline{B})}})} + \overline{(\overline{D} + \overline{\overline{(\overline{C} + \overline{A})}})})}}$$

Draw the circuit.

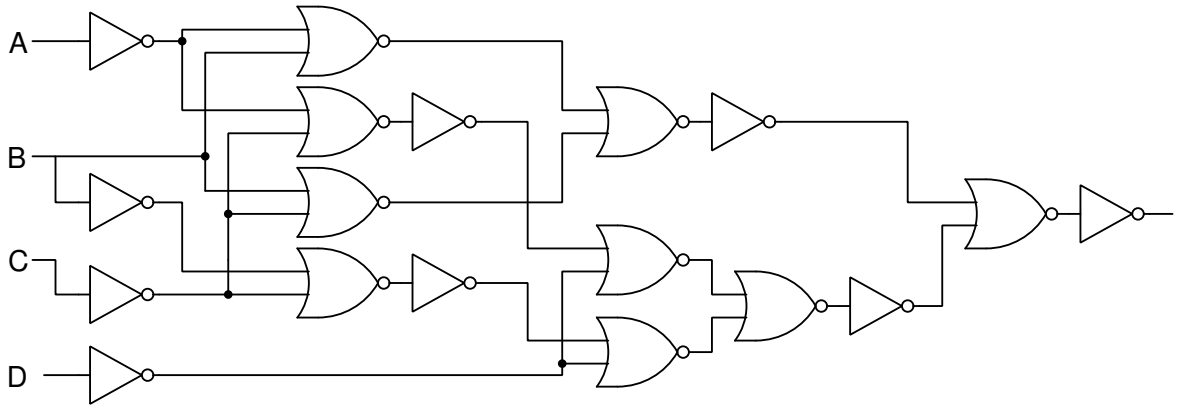


Figure 14: The 2 input NOR and INV gates circuit variant2.

Remarks

The use of the Morgan's laws for the translation of arbitrary logic functions to NAND and NOR logic was extensively covered in the lecture (both in graphical and algebraic form). Exercises 24.12 (part of the tutorial assignments of week 6) and 24.13 (solution provided in week 6) provide the basis for applying the De Morgan's laws to Boolean expressions.

Point c

Analyse your given 2 input NAND, AND and NOR gates,
NAND2: $\overline{\overline{A} \cdot B}$
AND2: $\underline{A \cdot B}$
NOR2: $\overline{\overline{A} + B}$
and what you are after (a 2 input XOR expression): $(\overline{A} \cdot B) + (\overline{B} \cdot A)$
The first obvious observation is that the AND2 gate is not useful and can be ignored.

Variant 1

Pairing the NAND2 with an inverter provides $(\overline{A} \cdot B)$, which is half of the XOR expression. The NOR2 provides the other half $(\overline{B} \cdot A)$, using input inversion (already available in the circuit diagram). An additional 2 input OR gate is used to implement the OR of these two terms.

choose an OR2 to connect them and you are done.

A	$\overline{A}$	B	$\overline{B}$	$\overline{\overline{A} \cdot B}$	$\overline{\overline{\overline{A} \cdot B}}$	$\overline{\overline{A} + B}$	$\overline{B} \cdot A$	$\overline{A} \cdot B + \overline{B} \cdot A$
0	1	0	1	1	0	0	0	0
0	1	1	0	0	1	0	0	1
1	0	0	1	1	0	1	1	1
1	0	1	0	1	0	0	0	0

Variant 2

See that the NAND2 is only zero for the first term of your XOR2: $(\overline{A} \cdot B)$. Adding an inversion to the NOR2 gives you zero only for the second term $(\overline{B} \cdot A)$. If you connect both of them to an AND2 you get an XNOR2 function, but if you use an NAND2 you have a XOR2.

A	$\overline{A}$	B	$\overline{B}$	$\overline{\overline{A} \cdot B}$	$\overline{\overline{A} + B}$	$\overline{\overline{A} + B}$	$\overline{\overline{\overline{A} \cdot B} \cdot \overline{\overline{A} + B}}$
0	1	0	1	1	0	1	0
0	1	1	0	0	0	1	1
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	0

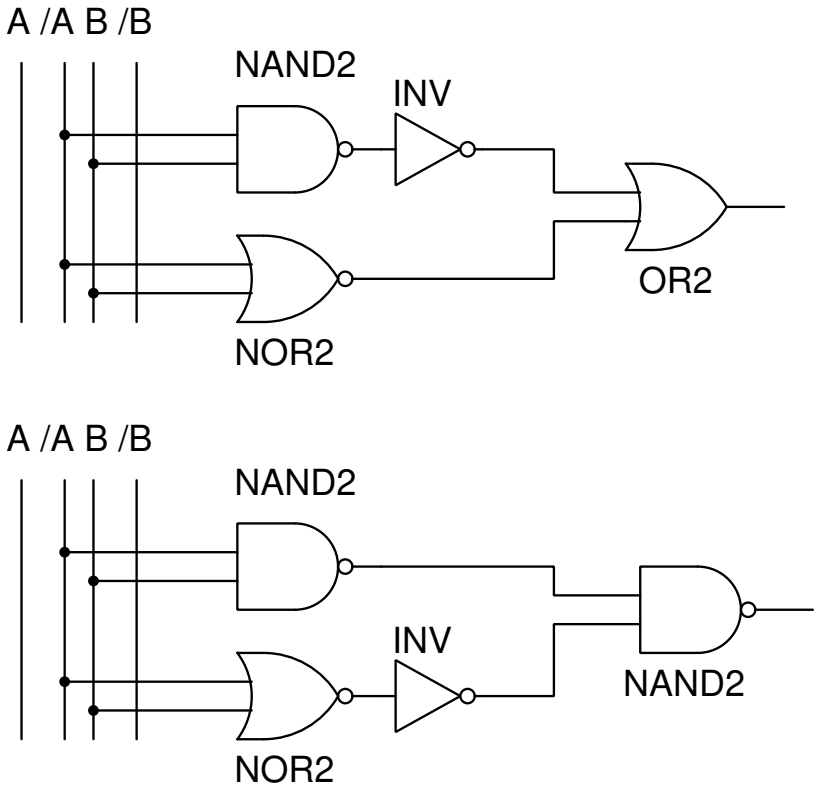


Figure 15: The XOR2 circuit.

Remarks

The skill set needed to approach exercise 24.19 is the same required to solve this question.